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AND preload OR overlap "floating point regis - 2003 Search

The "AND" operator is unnecessary -- we include all search terms by default. [details]

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[PDF] ▶An Efficient Algorithm for Exploiting Multiple Arithmetic Units
RM Tomasulo - IBM Journal of Research and Development, 1967 - courses.ece.uiuc.edu
... This sequence illus- trates the cardinal precedence principle: No floating- point register may participate ... Now overlap is impossible and the program ...
Cited by 733 - Related articles - View as HTML - Web Search - All 25 versions

Integrating register allocation and instruction scheduling for RISCs
DG Bradlee, SJ Eggers, RR Henry - Proceedings of the fourth international conference on ..., 1991 - portal.acm.org
... additional register is used, then they can overlap (b). Assuming a 4-cycle multiply, schedule (b) takes 4 fewer cycles. shown. Assuming no cache misses and a 2 ...
Cited by 160 - Related articles - Web Search - Library Search - All 2 versions

The MIPS R10000 Superscalar Microprocessor - ▶toronto.edu [PDF]
KC Yeager - 1996 - doi.ieeecomputersociety.org
... single- or double-precision formats in the floating-point register file ... 13 Clocks and output drivers ... secondary-cache data buffer to reduce overlap current spikes ...
Cited by 623 - Related articles - Web Search - BL Direct - All 14 versions

A pipelined interface for high floating-point performance with precise exceptions.
S Iacobovici - IEEE Micro, 1988 - doi.ieeecomputersociety.org
... floating-point instruction-execution overlap becomes less ... of floating-point and integer instructions ... in- structions with floating-point register destinations. ...
Cited by 15 - Related articles - Web Search - All 5 versions

The Visual Instruction Set (VIS) in UltraSPARCm
L Kohn, G Maturana, M Tremblay, A Prabhu, G Zyner - Proceedings of the 40th IEEE Computer Society International ..., 1995 - doi.ieeecs.org
... on the enclosing cube into the floating point register file, It assmnes 16 bits ... the destination address is aligned to a 64byte boundary, and preload the source ...
Cited by 104 - Related articles - Web Search - BL Direct - All 6 versions

Developing the WTL 3170/3171 Sparc floating-point coprocessors
M Birman, A Samuels, G Chu, T Chuk, L Hu, J McLeod ... - IEEE Micro, 1990 - doi.ieeecomputersociety.org
... to integrate all float- ing-point controller functions; floating-point register file; and ... 170 and 3 17 1 allow a multiply and an add operation to overlap. ...
Cited by 28 - Related articles - Web Search - All 5 versions

The Alpha 21264 microprocessor architecture
RE Kessler, EJ McLellan, DA Webb - Computer Design: VLSI in Computers and Processors, 1998 ..., 1998 - ieeexplore.ieee.org
... Floating- Point Register Rename ... prefetch the associated (64-byte) cache blocks to overlap the cache ... can also eliminate unnecessary data reads, and control cache ...
Cited by 216 - Related articles - Web Search - All 2 versions

ON THE FLOATING POINT PERFORMANCE OF THE r860™ MICROPROCESSOR

K LEE - International Journal of High Speed Computing, 1992 - worldscinet.com
... per second and a vector operation is, in this case, a load of a floating point register. ...
If source and destination vectors overlap we may not get ...
Cited by 24 - Related articles - Web Search

Floating point arithmetic two cycle data flow

D Cocanougher, RK Montoye, M Nguyenphu, SL Runyon - US Patent 4,999,802, 1991 - freepatentsonline.com
... and add alignment steps 104 and 106 respectively overlap. ... Steps 108 and 110 are referred
to as the ... result in written into the floating point register file 10. ...
Cited by 17 - Related articles - Web Search - All 4 versions

A unified vector/scalar floating-point architecture

NP Jouppi, J Bertoni, DW Wall - ACM SIGARCH Computer Architecture News, 1989 - portal.acm.org
... architecture provides a single unified vector/scalar floating-point register file ...
or stores were honored, most useful overlap of transfers and computa- tions ...
Cited by 18 - Related articles - Web Search - Library Search - All 5 versions

Key authors: R Tomasulo - K Yeager - R Kessler - E McLellan - D Weaver

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